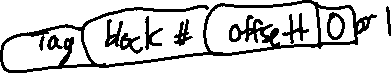
TPS:

1. Cache pronounced cash is a small fast on chip memory in which copies of items are kept in cache for fast subsequent access. We need a cache to increase performance and to hold data and instructions which are retrieved from DRAM to provide faster access to the CPU.
2. No Questions asked
3. No Questions asked
4. Offset of 4 bits (log 2 n)
5. 6 = log 2 (number of blocks in cache)
6. 1KB
7. Tag bits gets the left overs of index and offset. Cache and ram can have the same address
8. 1. Main memory is 2^20
   2. 3 bits
   3. 16 block
   4. 4 bits
   5. 13 tag bits



* 1. 4 bits

**Assignment Cache in your computer**

1. This surface pro 6 has (L1 Instruction,L1 Data,L2,L3) so yes there is a separate cache for data and instruction.
2. Each level of cache from L1 Data to L3 is (4x32 KBytes, 4x32 KBytes, 4x256 KBytes, 8 MBytes)
3. Line size from L1 Data to L3 is (64 bytes line size, 64 bytes line size, 64 bytes line size, 64 bytes line size)
4. (8 way,8 way,4 way, 16 way)
5. L1 Data cache there are:

Tag bits: 8 GB

Index bits: 6 bits

Offset bits: 6 bits